RL-TR-96-217
In-House Report
March 1997

METAL-SEMICONDUCTOR-METAL PHOTODETECTORS FOR OPTICAL INTERCONNECT APPLICATIONS

Franz Haas

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Rome Laboratory
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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	March 1997	**FINAL, Oct 91 - Sep 95** (In-House)

4. TITLE AND SUBTITLE
METAL-SEMICONDUCTOR-METAL PHOTODETECTORS FOR OPTICAL INTERCONNECT APPLICATIONS

5. FUNDING NUMBERS
C - NA
PE - 62702F
PR - 4600
TA - P3
WU - 24

6. AUTHOR(S)
Franz Haas

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Rome Laboratory/OCPA
25 Electronic Pky
Rome NY 13441-4515

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory/OCPA
25 Electronic Pky
Rome NY 13441-4515

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
RL-TR-96-217

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: Franz Haas, OCPA, (315) 330-2131

12a. DISTRIBUTION AVAILABILITY STATEMENT
APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

A method of lowering the dark current of silicon metal-semiconductor-metal (MSM) photodetectors was developed. MSM photodetectors have been the focus of much recent research. The monolithic design, integratability with standard VLSI circuitry, high speed performance, and applicability to 2-D array layouts make them a good candidate for optical interconnect architectures. In many optical interconnect schemes, the combination of low optical power emission from optical sources, low cost and low efficiency optical guiding or focusing systems and realistic alignment limitations often result in low optical signal level reaching the photodetector. To maintain an adequate signal to noise ratio for high data rates, the noise contributed by each component in the interconnect scheme must be minimized. This report reviews MSM photodetector operating characteristics, fabrication, and an analysis of a method of reducing the detector dark current.

14. SUBJECT TERMS
photodetector arrays, optical interconnects

15. NUMBER OF PAGES
36

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	**UNCLASSIFIED**	**UNCLASSIFIED**	**UNLIMITED**

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1. Introduction

Designing a better data transport system for computer architectures has been the impetus behind the Optical Interconnects research at the Rome Laboratory Photonics Center. We define "better" as providing higher data rates, higher density, and greater numbers of interconnects in comparison to traditional electronic methods of circuit interconnection. As computer processors increase in operating speed and as computers decrease in size, the need for a small footprint yet high capacity data bus is greatly increased. The objective of the optical interconnect research at Rome Laboratory is to provide solutions to these interconnect issues by furthering optical device development and interconnect design to demonstrate the feasibility of this developing technology.

This report details an analysis of a photodetector array developed for two optical interconnect architectures under development at the Photonics Center. An array of detectors with high responsivity and low noise is required for the multichannel board-to-board interconnect architectures. The properties of the metal-semiconductor-metal (MSM) photodetector, the fabrication process, and an analysis of a design variation used to decrease dark current are reported. The photodetectors were fabricated at the Cornell Nanofabrication Facility at Cornell University by the author.

The MSM photodetector was chosen as a good candidate for use in our optical interconnect architectures due to the use of standard silicon (Si) substrates, the potential for high speed operation, and the applicability to 2D detector arrays[1,2]. This type of photodetector has been extensively used for wavelengths ranging from ultraviolet[3] to infra red[4] and is capable of extremely high speed data rates (>30GHz for crystalline Si[5] and >290 GHz for bulk GaAs[6] substrates).

2. Applications For Low Noise Photodetector Arrays

The detector arrays described in this report were designed for two optical interconnect architectures under development at the Photonics Center. In both cases the optical interconnect is used to transmit information between computer boards or multichip modules (MCM's). Multichip modules are a means of densely packing bare circuit die on a substrate that provides mechanical stability, thermal transport, inplane electrical connectivity, and a foundation for integration into a larger system structure. Optical interconnects can provide a higher number and density of interconnects between individual MCMs than traditional electrical interconnect methods. Due to the inherent capability of MCM's to combine die of different materials the high speed Si integrated circuit die can be placed next to the high data rate optical transmitter and receiver die typically made on GaAs substrates.

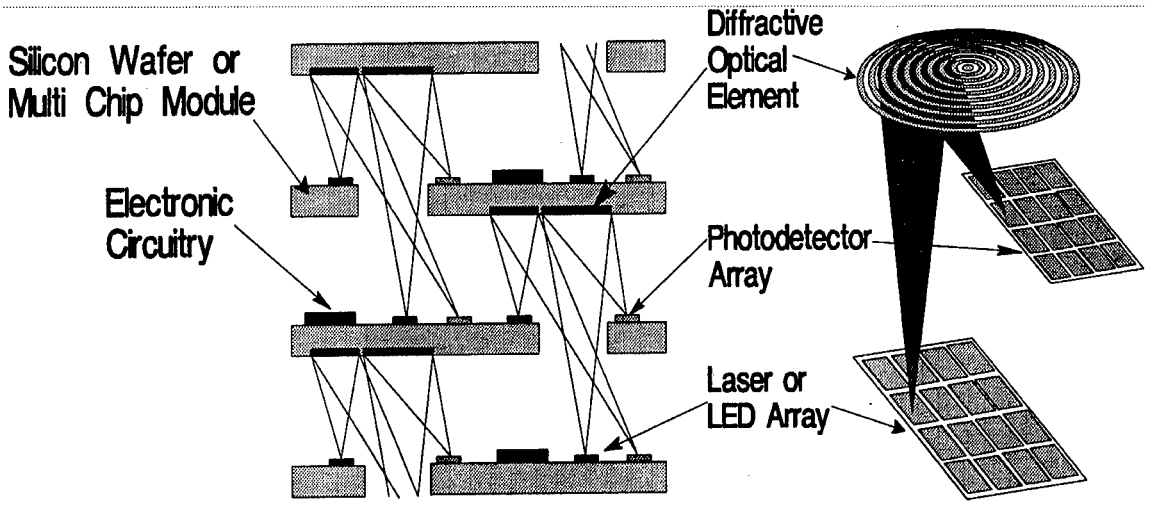


Figure 2-1. A board-to-board optical interconnect scheme based on arrays of LED's, photodetectors and an off-axis, reflective diffractive optic element.

Figure 2-1 depicts a plane-to-plane optical interconnect scheme based on an array of LED's, a diffractive optic element (DOE), and a photodetector array. The DOE redirects and focuses the LED array image onto the photodetector array. As its name implies, the DOE uses the diffraction of light off the mathematically defined etched structures to perform a complex optical function. The 1mm diameter DOE is etched by reactive ion etching (RIE) in Si and metalized to improve reflectivity. The LEDs are GaAsP homojunction diodes which emit at 655nm[7].

A second architecture, shown in Figure 2-2 in an expanded view, addresses the alignment difficulties and system costs associated with the above DOE-based architecture. Here, optical signals from one MCM are guided directly to detectors on a second MCM. LED's or vertical cavity surface emitting lasers (VCSEL's) can be used. A more detailed description of this architecture will be presented in the Final Technical Report for Rome Laboratory Project #4600P330.

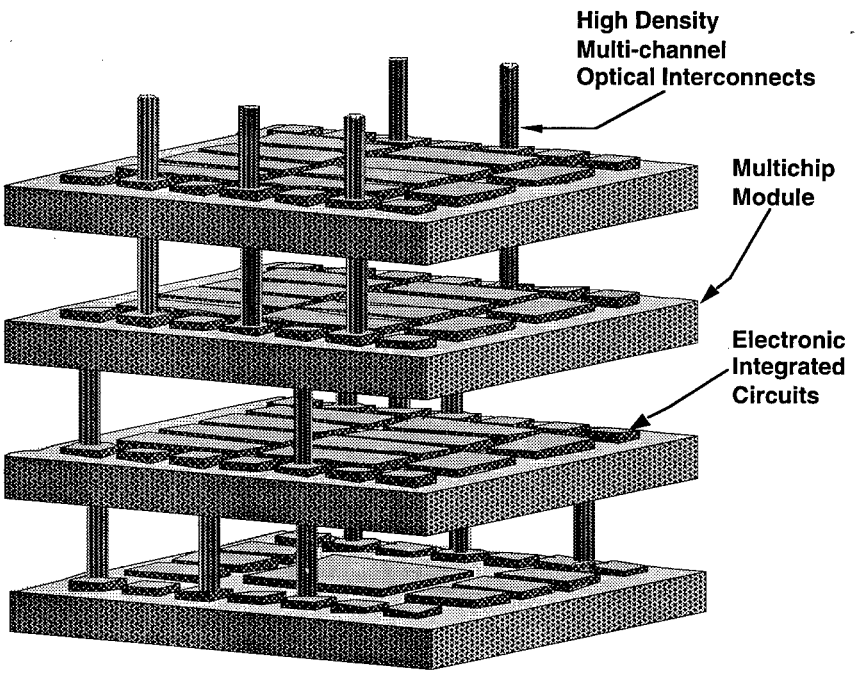


Figure 2-2. Multichip module (MCM)-to-MCM optical interconnect architecture.

3. MSM Photodetector Properties

Metal-semiconductor-metal (MSM) photodetectors have been the focus of much recent research. The monolithic design, integratability with standard VLSI circuitry, high speed performance, and applicability to 2-D array layouts make them a good candidate for optical interconnect components[2]. In many optical interconnect schemes, the combination of low optical power emission from optical sources, low cost and low efficiency optical guiding or focusing systems and realistic alignment limitations often result in a low optical signal level reaching the photodetector. To maintain an adequate signal to noise ratio for high data rates, the noise contributed by each component in the interconnect scheme must be minimized. The following section reviews MSM photodetector operating characteristics as well as an analysis of a method of reducing the detector dark current.

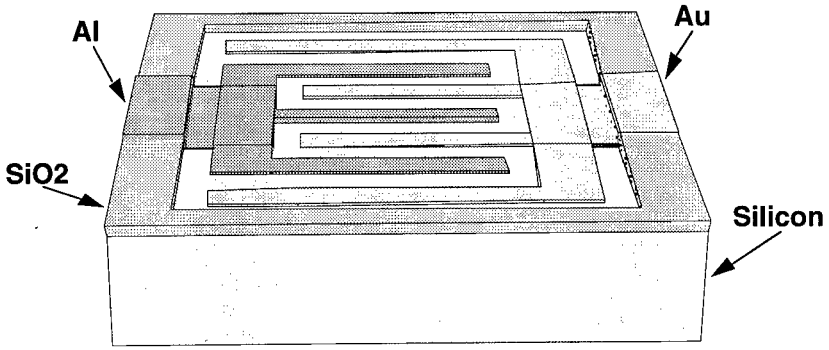


Figure 3-1. Metal-semiconductor-metal photodetector layout showing the Si active area, interdigitated metal electrodes, and the SiO_2 insulation.

MSM photodetector characteristics are determined primarily by substrate material, electrode metal, processing conditions, and electrode layout. The spectral responsivity of the detector is primarily a function of the substrate material band gap. Device operating speed is dependent on electrode geometry as well as substrate characteristics such as

electron and hole mobilities. Dark current is dependent on the characteristics of the rectifying contacts formed between the electrode metals and the substrate material.

Fundamentally, the MSM photodetector is comprised of a pair of biased interdigitated metalizations on a semiconductor surface (see Figure 3-1). The metal-to-semiconductor interfaces form Schottky or rectifying contacts. The combination of the two Schottky contacts create a low noise and highly sensitive photodetector, the physical properties of which will be explained in the following paragraphs.

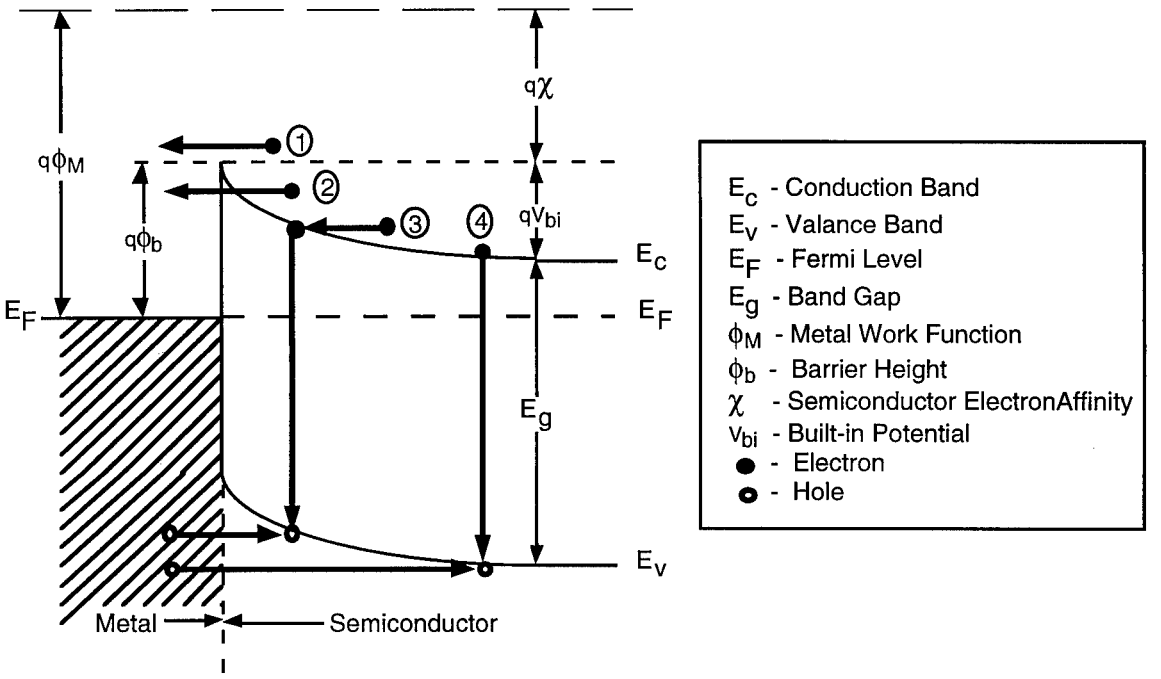


Figure 3-2. Energy diagram of a metal, n-type semiconductor contact showing carrier transport mechanisms[9].

The current transport processes responsible for both signal and dark current in MSM photodetectors are shown in the simplified metal-to-semiconductor interface energy diagram of Figure 3-2. This figure depicts the forward biased interface with the following carrier transport methods: (1) the transport of photo-generated electrons from the semiconductor to the metal over the potential barrier, (2) the quantum-mechanical tunneling

of electrons through the potential barrier, (3) the recombination of electron-hole pairs in the space-charged region, and (4) the hole injection from the metal to the semiconductor[8]. This report is concerned with the transport mechanisms labeled (1), the collection of photogenerated carriers which act as the desired signal and (4), the carriers injection from the metal into the semiconductor which contribute to the dark current.

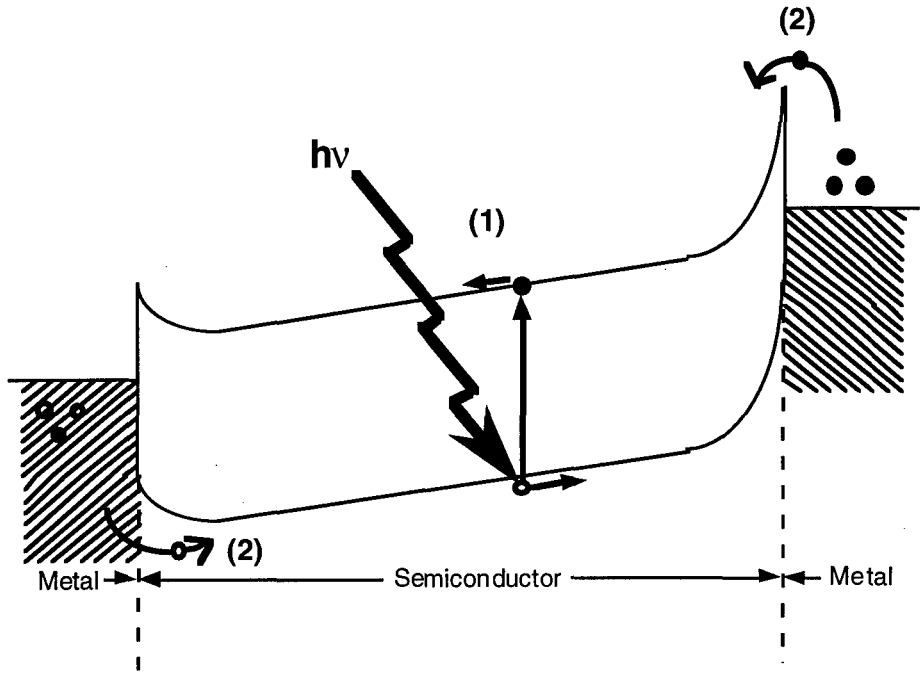


Figure 3-3. Energy-band diagram of a biased MSM detector indicating (1) the photogeneration of signal charges and (2) the thermally-generated carriers overcoming barrier heights adding to device dark current.

Figure 3-3 is an energy-band diagram of the MSM photodetector in the biased state. The vertical displacement of the electrode metals indicates the bias voltage applied to the device resulting in the forward biased condition of the left-hand metal-semiconductor interface and the reverse bias of the right-hand interface. Upon biasing, the Si between the electrodes becomes fully depleted of free carriers. The reversed biased interface prevents current from flowing through the device in the absence of an optical signal. The depleted regions between the electrodes are the photodetector active regions. A photon with a photon energy greater than the band gap of Si (1.12eV) will be absorbed by an electron exciting it to the

conduction band as shown by the process labeled as (1) in Figure 3-3. The photo-generated electron and hole are swept by the high applied fields to the positive and negative electrodes resulting in an electronic output signal.

As depicted in Figure 3-3 (labeled with a (2)) there is leakage current due to thermally excited carriers which make it over the barrier in the case of electrons (J_n) from the negative electrode and under the barrier in the case of holes (J_p) from the positive electrode[1]. The rate of flow of these carriers is determined by the size of the barrier that they encounter at the metal-to-semiconductor interface. In the case of electrons (a similar case can be made for holes) at the negative electrode, a certain percentage of electrons will possess the energy to overcome the barrier and enter the semiconductor and thereby add to the dark current of the system. The probability that an electron will have an energy, E can be approximated by the Fermi Function:

$$f(E) = \frac{1}{1 + \exp (E-E[f])/kT)} \cong \exp -(E-E[f])/kT)$$

for $E>(3kT + E[f])$ where E[f] is the Fermi energy, k is Boltzmann's constant, and T is temperature in degrees Kelvin. The number of electrons with energies greater than the barrier height decreases exponentially with the increase barrier height. Therefore, increases in barrier height can be used to decrease the detector dark current[9]. The current contribution of electrons emitted over the barrier from the metal to the semiconductor is defined by Bethe's thermionic emission theory:

$$J_{ms} = \frac{pqN_c(8kT/\pi m^*)^{1/2}}{4} \exp(-q\,\phi_b/kT)$$

where p is the fraction of electrons tunneling from the semiconductor to the metal, q is the electron charge, Nc is the effective density of states in the semiconductor conduction band, m* is the effective mass of electrons in the semiconductor, and ϕ_b is the metal-semiconductor interface barrier height. Again, we see that the current decreases exponentially with respect to increases in the barrier height[10].

The barrier height, ϕ_b , of the metal-semiconductor interface can be approximated from the electron affinity of the semiconductor, χ, (the energy needed to take an electron from the conduction band to vacuum), and the metal work function, ϕ_M, (the energy required to take an electron from the metal Fermi level to vacuum). This can be seen in the energy diagram of Figure 3-2 and is represented by the following equation (barrier lowering due to the Schottky effect is ignored here for simplicity):

$$\phi_b = \phi_M - \chi$$

The semiconductor affinity is a characteristic of the semiconductor material and doping, both factors are fixed by industry standards for low cost Si wafers. The choice of metals, and therefore, the choice of metal work functions is more variable. The main constraint on the choice of a metal is that it must form a rectifying contact with the semiconductor substrate. To meet this requirement the metal work function (ϕ_M) must be greater than the semiconductor work function (n-type Si with a doping level of $8X10^{14}$ cm^{-3} has a work function of 4.32eV).

A large value of ϕ_b will limit the number of thermally excited electrons which pass from the negative electrode to the semiconductor. Likewise a small ϕ_b value will result in a

greater barrier for holes passing from the positive electrode to the semiconductor. This can be seen in Figure 3-4, note that the semiconductor band gap E_g is a constant. If different metals are used for the positive and negative electrodes, then the barrier heights can be optimized to reduce the number of either electrons or holes which acquire enough energy to overcome the barrier thereby reducing the device dark current.

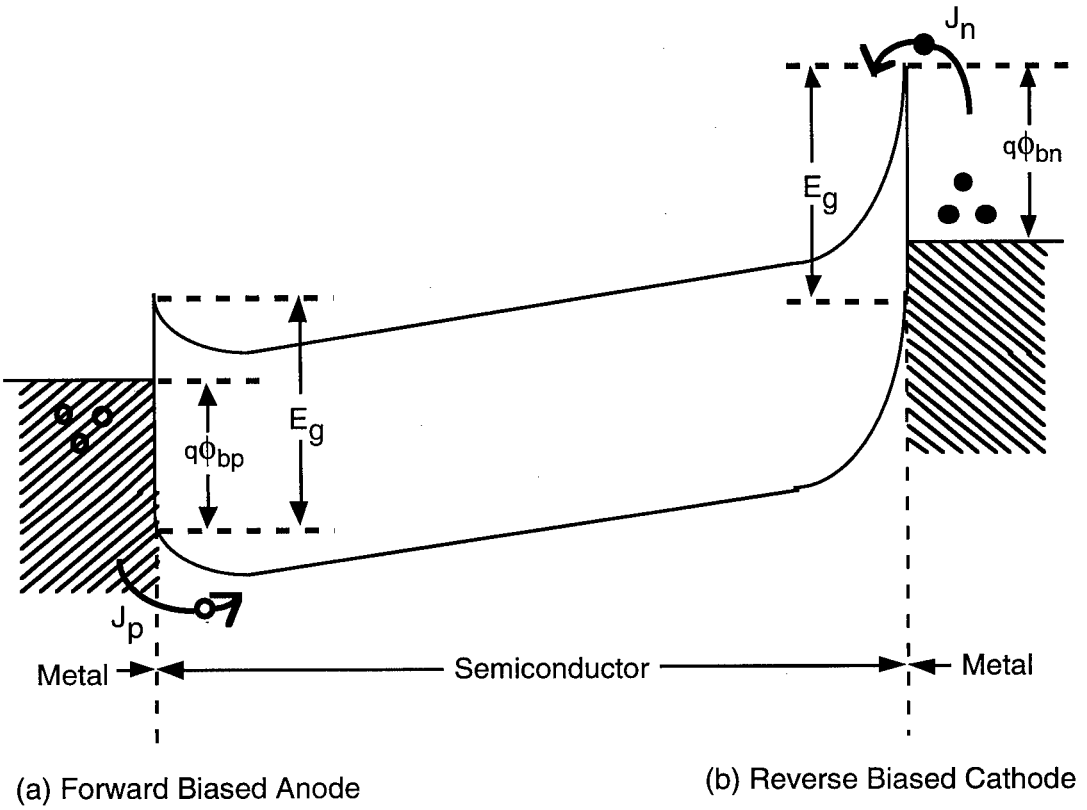


Figure 3-4. Energy band diagram of an MSM photodetector showing (a) the positive electrode, forward biased interface and (b) the negative electrode, reverse biased interface. Different metals form different barrier heights to prevent unwanted hole (J_p) or electron (J_n) transport into the semiconductor.

Aluminum (Al) and gold (Au) were chosen as the positive and negative detector electrodes, respectively. Both metals are common VLSI materials and have work functions greater than the Si work function of 4.32eV (4.55 for Al and 4.86 for Au). The barrier height for Al-Si interface is 0.50eV resulting in a 0.62eV barrier for the holes to pass "under". The Au-Si interface results in a 0.81eV barrier height for the electrons to pass "over".

The above description of the metal-semiconductor interface dynamics is, however, an idealized model. Three factors which may upset this model are the effects of surface states in the semiconductor, imprecise work function figures, and the presence of a significant interfacial layer. The presence of surface states in the semiconductor play a major role in dictating the location of the Fermi level at the metal-semiconductor interface. If the density of surface states is high, then the Fermi level will be "pinned" to an energy level determined by the doping of the semiconductor and the properties of the surface states and the Schottky barrier height will be defined by the following equation:

$$q\phi_b = (Eg - q\phi_o) - q\,\Delta\phi$$

Where ϕ_o is the energy level at the semiconductor surface which is heavily influenced by surface states and $\Delta\phi$ is the image force barrier lowering due to the Schottky effect[8]. Note that the barrier height is no longer influenced by the metal work function. The processing conditions used to clean the semiconductor surface before metal deposition play a major role in the creation of surface states.

The usefulness of the dual metal technique depends on the ability to "design" a barrier height by choosing a metal with a known work function for use in a Schottky barrier. Unfortunately, barrier height values vary greatly by the method of surface preparation, metal deposition, and the test environment[10]. Idealized values are obtained by cleaving semiconductors in vacuum and depositing metal onto the clean surface. The variation in surface cleaning and metal deposition technique between the researcher tabulating barrier height tables and the manufacturer of devices often results in differing results. It is not feasible to construct photodetectors under the idealized conditions used to determine the metal-semiconductor barrier height. Contamination of the surface due to wet chemical and air exposure results in increased surface states and the formation of an interfacial oxidation layer which results in further departure from the idealized model.

4. Fabrication

Standard silicon fabrication processes and equipment were used to design and fabricate the detector arrays. The following paragraphs detail the computer aided design (CAD), mask fabrication, and processing steps used to create the detectors. An outline of the main fabrication processes is given in Table 4-1. Some steps (i.e. the lift-off process to define metalizations) were repeated using different masks to define the various structures of the photodetectors.

TASK	PROCESS STEPS
CAD chip layout:	design layout pattern fracture
Mask Fabrication:	mask exposure mask development mask descum mask etch mask inspection
Metal definition (Lift-off):	vapor prime Si wafers photoresist spin hot bake exposure image reversal - NH_3 bake bulk UV exposure wafer develop wafer descum HF native oxide etch evaporation lift-off soak, ultrasound wafer inspection
SiO_2 growth:	wafer clean PECVD chamber clean PECVD oxide growth
SiO_2 etch:	vapor prime Si wafers photoresist spin hot bake exposure HF etch

Table 4-1. Outline of the main fabrication steps required for MSM photodetector processing. Repeated steps are not listed.

4.1. Chip Layout

The first step in fabricating a device is to draw out the patterns which represent the metalizations, isolation etch areas, alignment marks, bonding, etc... This "drawing" is literally a blueprint of the final chip. Each fabrication process is represented as a different mask layer in the computer aided design (CAD) drawing. The CAD program used was SYMBAD, a VAX-station based polygon editor which converts graphical data into a standard GDS (Graphic Data Stream) format. Six mask levels were defined: alignment marks/bonding pads, SiO_2 etch windows, metalization 1, metalization 2, Si etch, and soldier pads. A compilation of the six mask levels is shown in Figures 4-1 and 4-2.

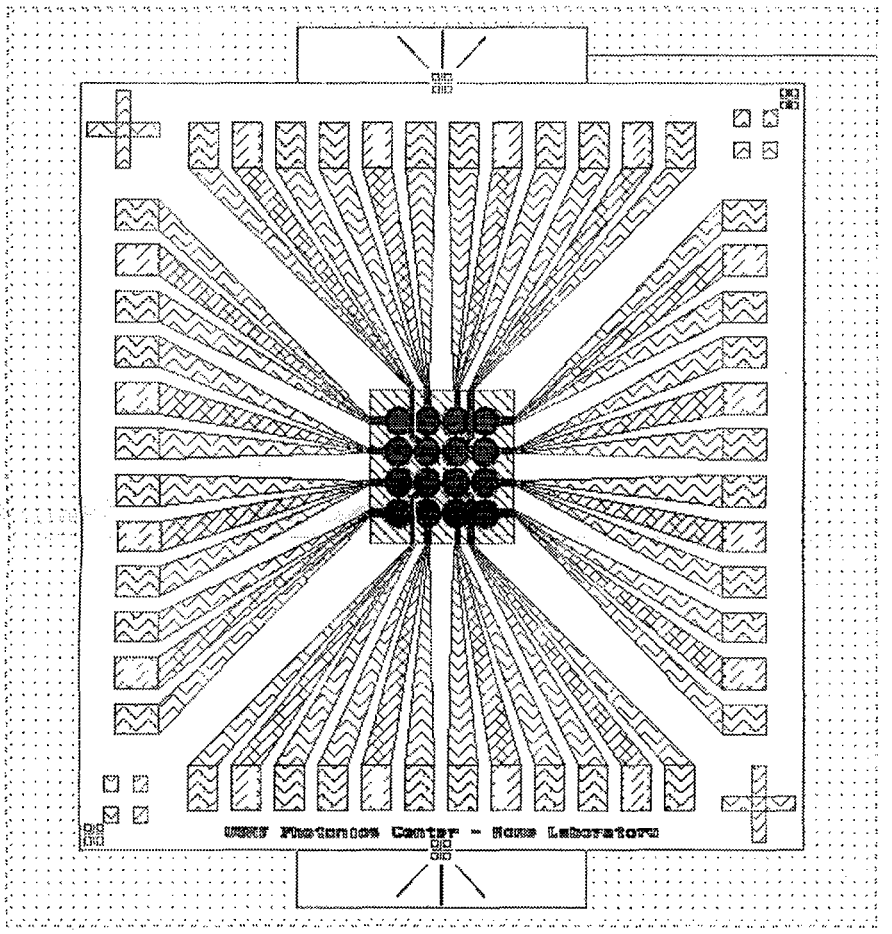
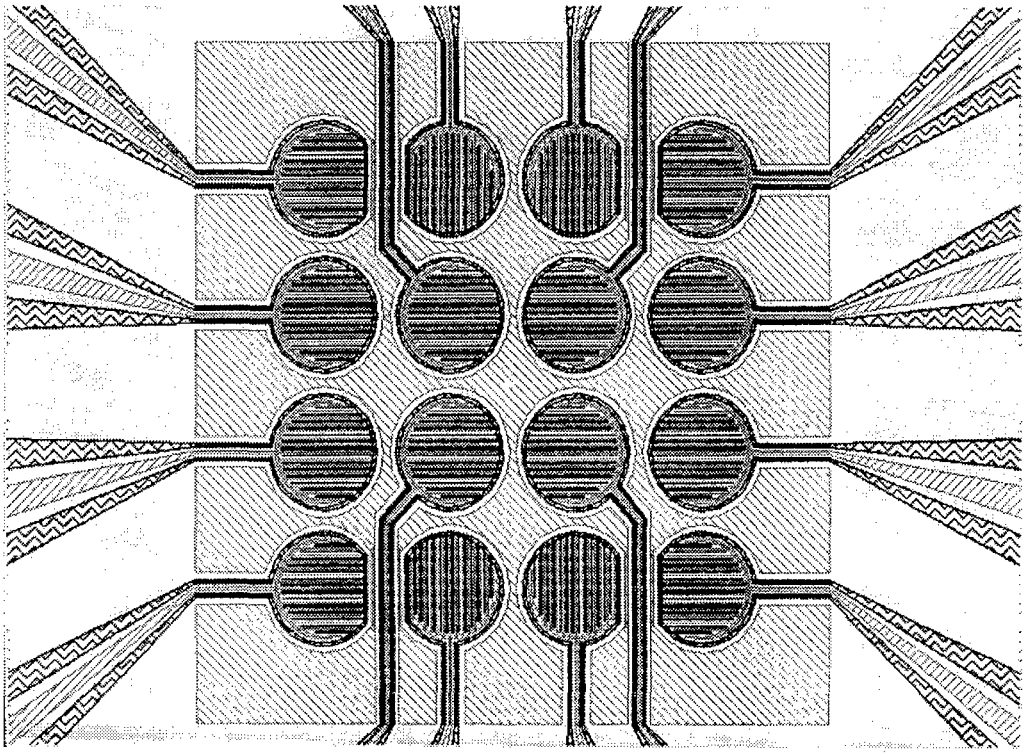


Figure 4-1. Overlay of six mask patterns which define the MSM detector chip.

(a)



(b)

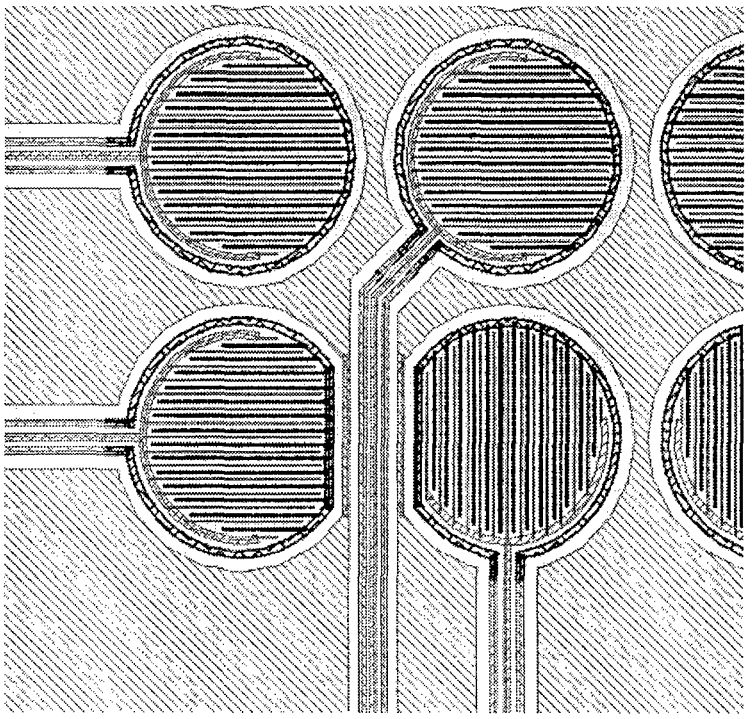


Figure 4-2. A close-up of the six mask overlay showing (a) the 4X4 detector array and (b) individual devices.

After the MSM detector chip was laid out, the graphical pattern was fractured into rotated rectilinear subunits required to drive the exposure aperture of the Pattern Generator used in exposing the masks. This function is performed by the DRACULA program.

4.2. Mask Fabrication

Five inch, chrome-on-glass masks with pre-spun photoresist were exposed using a GCA/MANN 3600F Pattern Generator. The Pattern Generator exposes the mask in piecemeal fashion using an rectilinear aperture which can be resized and rotated. Each rectilinear unit of the fractured CAD data is represented by a single move, rotate, resize of the aperture and exposure flash. A complicated CAD design can have as many as 10,000 flashes requiring approximately 4 hours of exposure time. The smallest aperture setting results in a 2μm exposure square on the mask .

After exposure the masks were developed for 1min in Shipley MF312 followed by a de-ionized water (DI H_2O) rinse. The developing process removes photoresist in areas that were exposed by the Pattern Generator. Masks with fine features (such as the detector electrode layer) were placed in a reactive ion etcher (RIE) and exposed to a short period of O_2 plasma in a "descum" process used to clear unwanted photoresist residue which may not have been cleared by the developing process. A Cr etch was used to dissolve the Cr not covered by photoresist. After a DI H_2O rinse and careful inspection to insure complete Cr etching, the remaining photoresist was removed by soaking the plate in Shipley MF965 Resist Strip for 1 hour. A final mask inspection was performed to insure correct pattern transfer, feature dimensions, and Cr etching.

4.3. SiO_2 Growth

As the first step in the detector processing, SiO_2 was thermally grown on twenty Si wafers. SiO_2 is used to isolate the bond pads and non-detector metalizations from the conductive Si surface. The wafers were subjected to a high temperature resulting in the oxidation of the exposed Si surface. Ten wafers were grown with 1000Å of SiO_2 and ten were grown with 2000Å of SiO_2.

4.4. Photolithography

The first level metalization was patterned using a standard liftoff process. This level included alignment marks needed for the alignment of future mask steps and an adhesion layer for all metalizations excluding the detector active areas. Cr, used for this layer, forms a stronger bond with SiO_2 and Si than Au or Al (the metals used to define the detector electrodes). Cr is well suited for alignment marks because it contrasts well with Si and SiO_2 when viewed through the stepper alignment microscope and camera system.

Standard 3inch N-type Si wafers were used as the detector substrate. All wafers were vapor primed by baking in an HMDS atmosphere for 34min prior to application of phototresist to aid in resist adhesion. KTI 895i-16cs positive photoresist was spun at 3000rpm for 30sec giving a resist thickness of 1.5microns. The photoresist solvents were then evaporated by a 90°C hot plate bake for 60sec.

A GCA/MANN 4800 10:1 Stepper was used to expose the wafers with a reduced image of the mask pattern. The resulting die size was 6mmX6mm which was replicated or "stepped" across the wafer 112 times. The Stepper has an i-line light source emitting at 365nm with a resolution limit of 0.5nm and a layer-to-layer alignment of less than one

micron. Each mask was characterized by conducting an exposure/focus test run with the Stepper to determine the ideal exposure time and machine focus setting which varies for mask pattern and resist characteristics (i.e. thickness, manufacturer, age etc...).

4.5. The Lift-off Process

Two fabrication processes were used to define detector structures, liftoff for metal patterning, and etching (wet and dry) for SiO_2 and Si removal. Liftoff allows for the definition of extremely small structure dimensions (less than one micron). After vapor priming, photoresist spin, and hotplate bake the wafers are exposed using the GCA/Mann 4800 Stepper in areas where metal will NOT remain. The wafers are then baked in an NH_3 ambient for 80min at 90°C which "fixes" the exposed resist leaving the unexposed resist unaffected. The wafers are then exposed for 30sec under a UV light source (an HCG Contact Aligner was used in the bulk expose mode with g-line 450nm light) affecting only the resist that was originally unexposed using the Stepper. This process "reverses" the positive photoresist - making the originally exposed photoresist stay after development and the originally unexposed areas dissolve during development. The remaining photoresist will have an edge slope profile inverse of a "normally" developed positive photoresist (the liftoff procedure is graphically outlined in Figure 4-3). This edge profile allows for very small dimension metalizations and etches.

After the bulk UV exposure the wafers were developed for 60sec in Shipley MF312 followed by a DI H_2O rinse. A wafer descum was performed in a Branson Barrel etcher using an O_2 plasma at 500W of RF power for 0.5 min. Metal was evaporated using a thermal evaporator pumped down to 2X10-7 Torr. Metal evaporation is a line-of-site deposition system, the metal ingots are raised just above their melting points, evaporating a

uniform thickness of metal onto the wafers. Thickness monitors inside the evaporation chamber monitor deposition rates.

The wafers were then soaked for up to 24 hours in Shipley MF965 Resist Strip to complete the liftoff process. The edge slope profile created by the "image reversal" process allows the resist strip to flow under the unwanted metal and dissolve the photoresist supporting it. Metal remained on the Si in the areas originally not exposed by the initial Stepper exposure process. In cases where the liftoff process was incomplete leaving metal covered photoresist, the wafers were subjected to a 10 to 30sec of ultrasound while in a bath of acetone followed by a isopropanol rinse and blown dry using pressurized N_2.

4.6. SiO_2 Etching

After the alignment marks were in place, windows in the SiO_2 were etched down to the Si to define the photodetector active areas. The wafers were again subjected to an HMDS vapor prime, coated with photoresist (KTI 895i-16cs spun at 3000RPM for 30sec), followed by a 60sec hotplate bake at 90°C. A focus/exposure test of this mask resulted in an optimum stepper setting of a focus of 251 and an exposure time of 1.2sec. After exposure the wafers were developed in OCG developer MFR321 for 90sec. followed by a DI H_2O bath.

The photolithography and resist development process left the SiO_2 exposed only in areas illuminated by the stepper. In these areas the SiO_2 was removed to the Si substrate by soaking in a buffered 6:1 hydrofluoric acid (HF) solution for 2min for the wafers coated with 1000Å of SiO_2 and 3min for the wafers coated with 2000Å of SiO_2. The 6:1 HF solution is an excellent SiO_2 etch due to the large contrast in etch rate of SiO_2 (1200Å/min for thermally grown SiO_2) and Si. The completion of the etch is easily determined by the beading of the HF solution on the exposed Si. Care should be taken when using HF as it

is extremely toxic, it is readily absorbed through the skin, and it can not be stored in glass containers (HF is used to etch SiO_2). A two-staged DI H_2O rinse was used to neutralize the residue of this strong acid followed by a spin drying process.

4.7. Electrode Definition

Up to this point alignment marks and a metalization adhesion layer were defined and widows in the SiO_2 isolation layer were etched to expose bare Si for the detector active areas. The next step was to create the 1μm wide detector electrodes which collect the photogenerated charges. The lift-off process described above for the alignment marks was repeated twice, once for the detector cathode (Au) and once for the anode (Al). An additional cleaning step was added prior to the deposition of the electrode metals. The wafers were dipped for 3-5sec in a buffered hydrofluoric acid (HF) 6:1 solution to remove native oxides on the Si surface to ensure an intimate metal-to-semiconductor interface.

4.7.1. Electrode Fabrication Enhancement

A variation in the process used to fabricate the detector electrodes negated the need for the SiO_2 etch mask step and produced devices with better responsivity. The electrode lift-off pattern was defined by the photoresist "reversal" process (defined above) directly onto the SiO_2 over the detector active areas. After resist development and descum, the wafers were subjected to a buffered HF SiO_2 etch to expose the Si only where the electrodes were to be deposited. The wafers were rinsed in DI H_2O, dried on a spinner, and quickly placed under vacuum to prevent excessive Si oxidation. Electrode metalizations were then deposited by thermal evaporation into the resulting "trenches" in the SiO_2 formed by the HF etch. Both the standard and modified lift-off process is outlined in Figure 4-3.

This technique has a number of advantages over exposing the entire detector active area. A quarter-wave (of the incident light) thick layer of SiO_2 will act as an anti-reflection coating increasing the detector efficiency. Uncoated, the Si surface reflects 30% of the incident light. This coating also serves to seal and passivate the Si surface making the detector performance more uniform over time and over a greater range of environmental conditions. The quarter wave thickness, D, for a specific material is calculated by:

$$D = \frac{\lambda}{n\,4}$$

Where λ is the operating wavelength of light and n is the refractive index of the coating material. The refractive index of thermally grown SiO_2 is 1.46 giving a quarter-wave thickness of 1122Å for 655nm light and 1455Å for 850nm light.

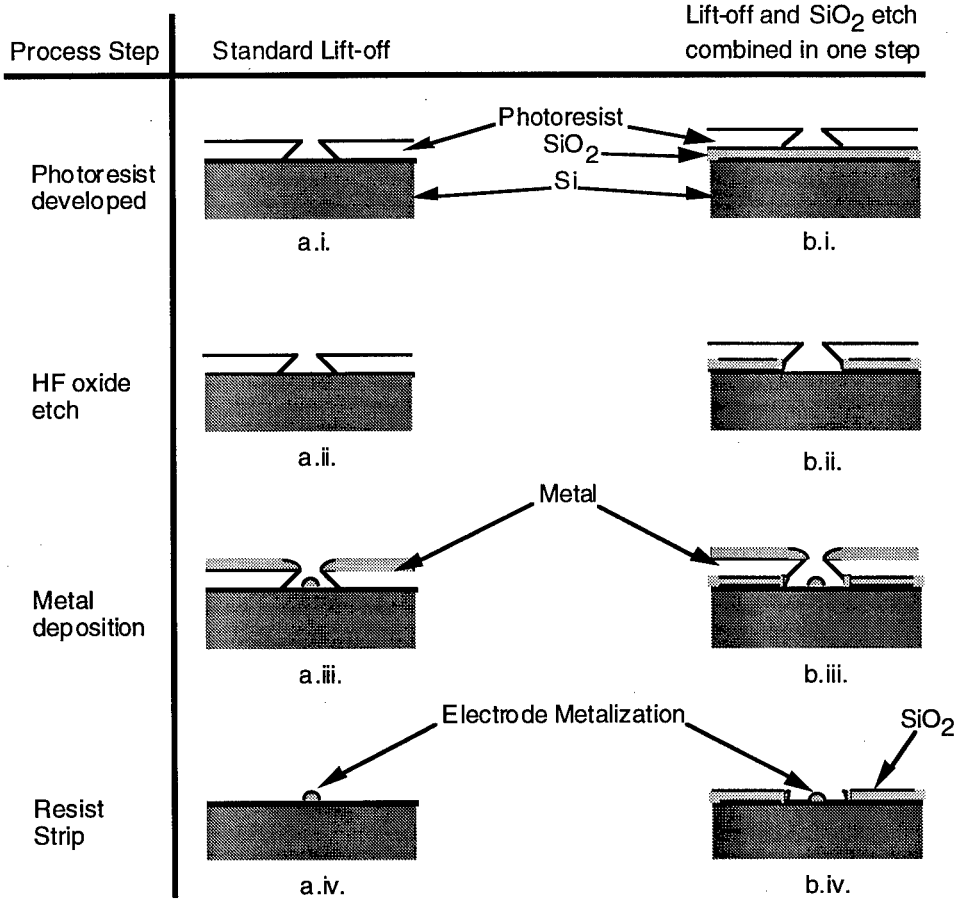
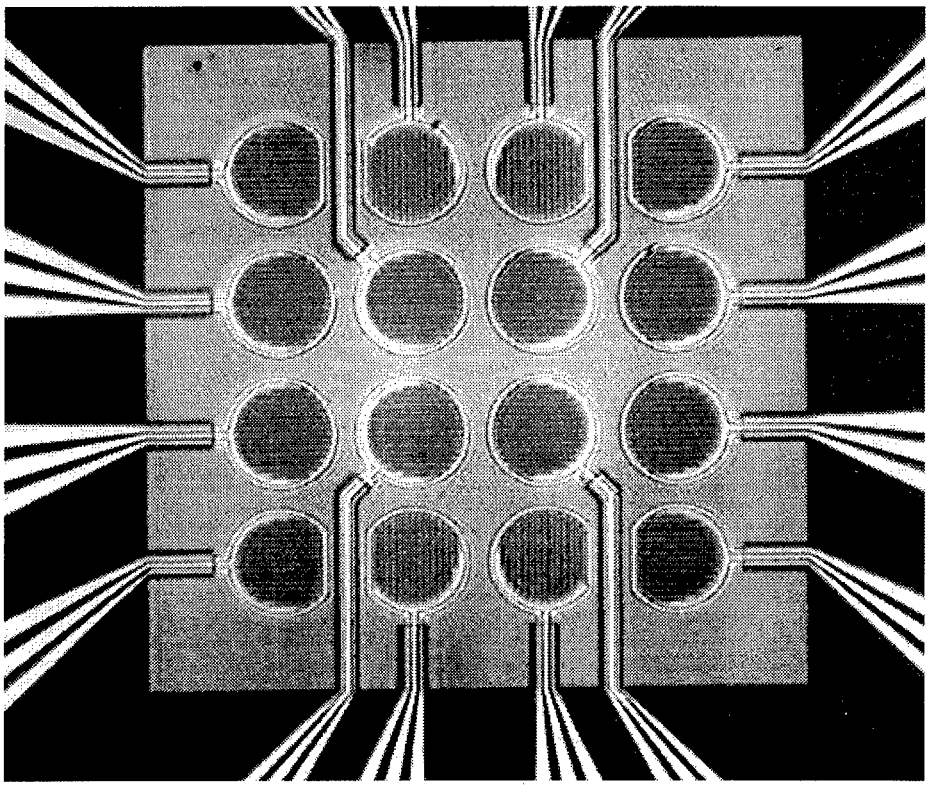
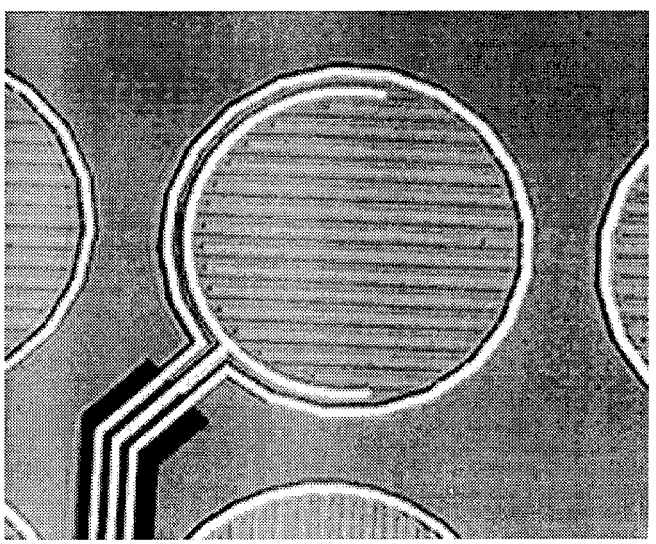


Figure 4-3. Two variations on the lift-off process for fine metalization definition are presented here. The process on the right combines an SiO_2 etch process with the metal lift-off.

(a)



(b)



(c)

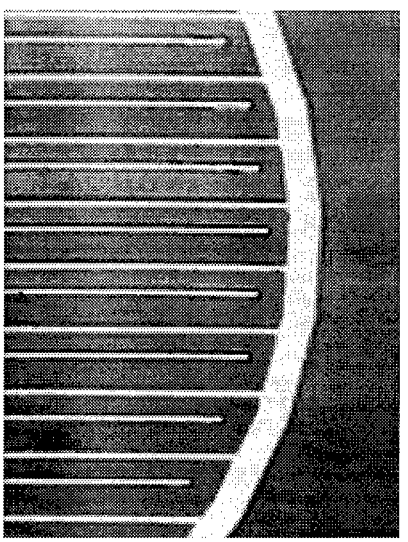


Figure 4-4. Optical micrographs of (a) MSM photodetector array, (b) a single device, and (c) a close-up of the interdigitated electrodes. The electrodes are 1μm wide with 4μm spaces between electrodes.

Methods of electronically isolating individual devices in the array were not accomplished at the time of this report. Proton bombardment and deep trench etching will be explored as possible solutions. The depth of the isolation structure (induced crystal defects by proton bombardment or removal of Si by reactive ion etching) must be great enough to prevent stray light intended for one detector to be collected by another.

5. Testing

An Anritsu 1445B semiconductor parameter analyzer was used to apply a voltage bias and measure the current output from the detectors. The detectors were supplied an optical signal from an optical fiber probe assembly. The output from a GaAs laser diode emitting at 780nm was launched into an optical fiber. A 3dB fiber splitter was spliced onto the fiber allowing one fiber to deliver optical signals to the device under test and the other fiber was used as an optical power monitor to determine the optical power delivered to the detector. The fiber output underfilled the detector active area.

Current-voltage (IV) plots for the MSM photodetectors are presented in Figure 5-1 for a range of input optical intensities. Figure 5-1 (a) shows the detector in the normal operating mode with the Al electrodes serving as the device anode and Au serving as the cathode. The plot shown in Figure 5-1 (b) shows the device operated with the bias on the electrodes switched.

Dark current IV curves are presented in Figure 5-2 for both the normal and "reverse" biased state of the device. The significant difference in dark current suggesting a strong dependence on metal used for anode and cathode. A dark current of 165pA at 3V bias was measured for the Al-anode, Au-cathode configuration.

Responsivity values of 0.32A/W were measured for the photodetectors with uncoated active areas. Devices coated with 1000Å and 2000Å of SiO_2 showed responsivities of 0.37A/W and 0.35A/W respectively. All three measurements were taken with 40μW of optical input.

6. Conclusion

The design, fabrication and test data on a photodetector array design used for optical interconnect applications has been presented. A method of reducing dark current has explored in device design, in the fabricating complexity of an additional mask and lift-off step, and in the resulting low dark current measurements. Also presented was a variation in the fabrication of the MSM electrodes which maintained the SiO_2 coating between the interdigitated electrodes which resulted in better device responsivity while decreasing the number of fabrication steps. Both the SiO_2 etch and a final antireflection coating step were avoided. Care in applying the initial SiO_2 coating thickness to obtain a quarter wave condition could greatly enhance detector performance.

The payoff of the two-metal electrode design to a specific application will be dependent on a range of issues including the amount of optical signal reaching the detectors, the temperature that the detector will be subjected to (increases in temperature will greatly increase dark current effects[11]), the importance of limiting DC currents to limit heating or other current induced noise effects[11], as well as the fabrication constraints. The current reduction may be worth the cost of an additional fabrication process if the detectors are operated at high temperatures or if extremely low optical signals are expected. Though it should be noted that certain materials and processes are more susceptible to surface state contamination which may dominate the determination of the interface barrier height.

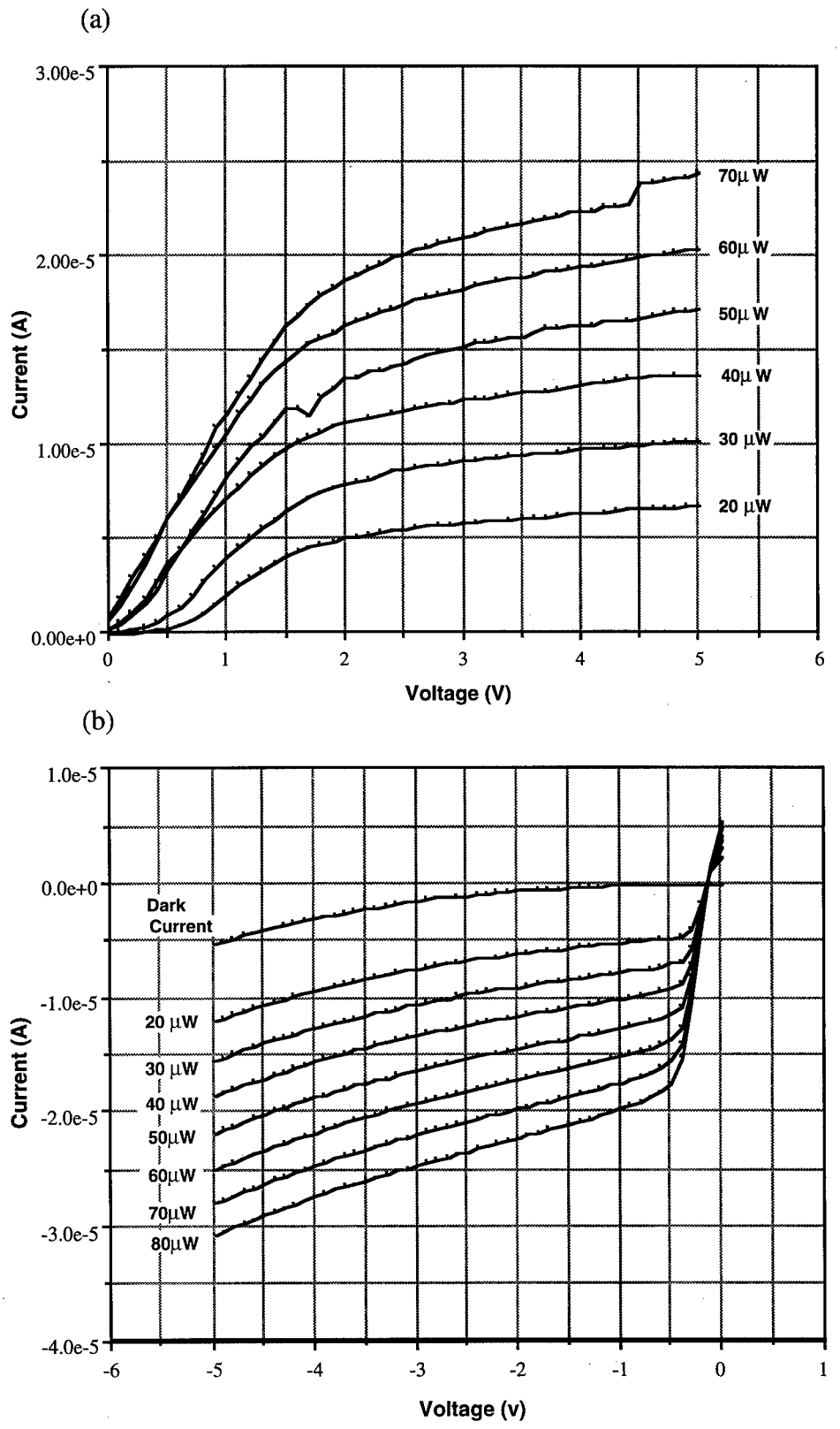


Figure 5-1. Current-voltage (IV) curves of a Si dual-metal MSM photodetector for a range of optical inputs. The plot labeled (a) shows the detector in the normal operating mode and in (b) the anode and cathode connections are swapped.

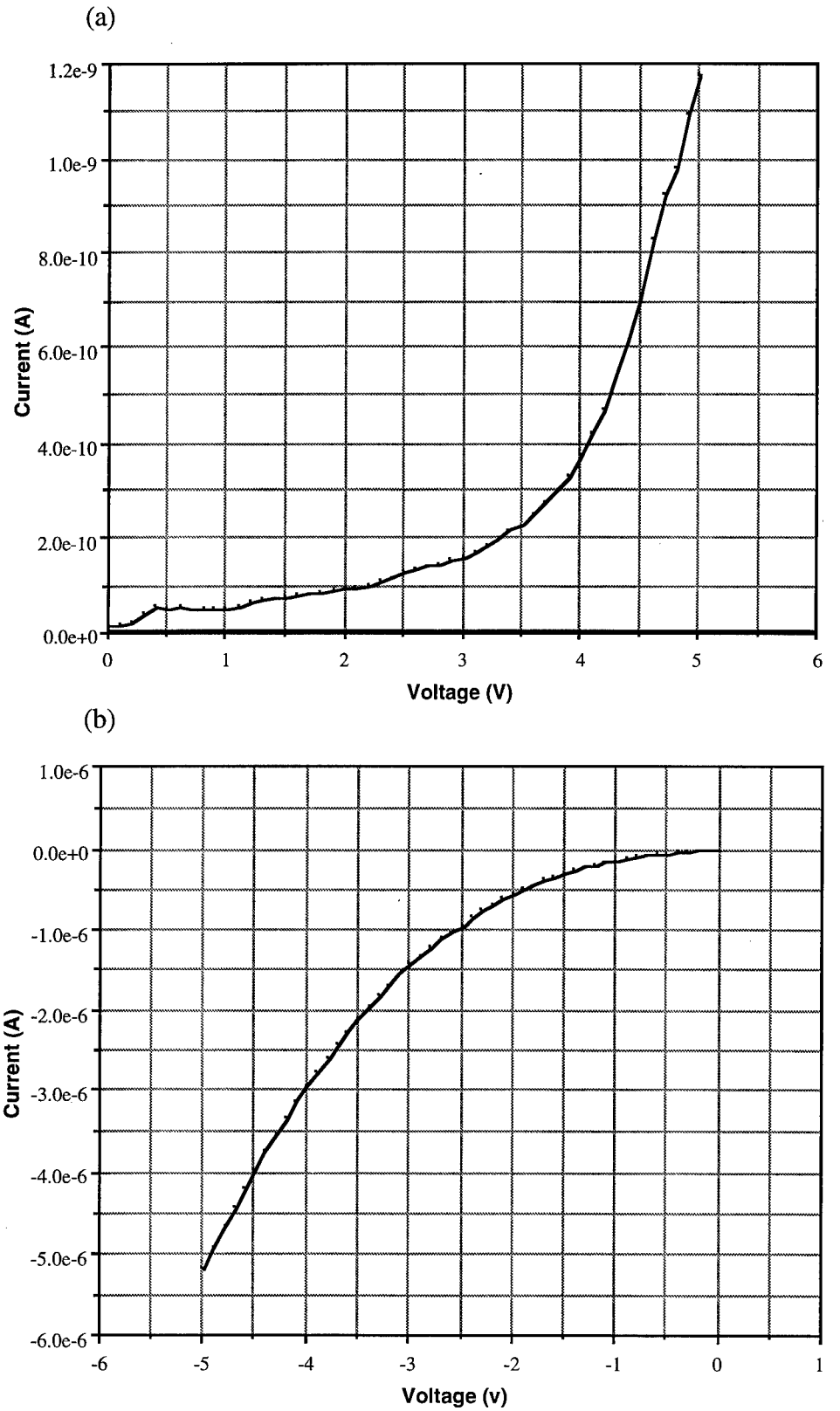


Figure 5-2. Dark current vs. bias voltage for the dual-metal MSM photodetector operated in the normal biased mode (a) and the photodetector operated with the anode and cathode connections switched (b).

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